REMARKS

Claims 1-30 are pending.

Claim 1 has been amended to correct the consecutive occurrence of the word "wherein".

No new matter is being added.

On page 2 of the Office Action, claims 1 is objected to because of the informality of reading: "a regulator; wherein wherein the memory …". Applicants have corrected claim 1 in order to remove the second occurrence of the word "wherein", thereby rendering this objection moot. Applicants wish to thank the Examiner for pointing out this typographical error.

On page 2 of the Office Action, claims 1-4, 6-8 and 9 are currently rejected under 35 USC § 103(a) as being unpatentable over US 5,847,552 (hereinafter referred to as "Brown") in view of US 6,484,265 (hereinafter referred to as "Borkar et al."). Applicants are traversing this rejection.

The application presently contains four independent claims, namely claims 1, 9, 20, and 30. Below, Applicants explain that Brown in combination with Borkar et al. do not teach all of the elements of claims 1 and 9.

Cited Brown concerns integrated circuit semiconductor chips that are subject to process variations, which can affect the operating parameters thereof (col. 1, lines 19-21). Brown suggests that the lower operating voltages of microprocessors and increased complexity thereof mean that the impact of process variations has become increasingly important (col. 1, lines 42-44).

As described at col. 3, lines 9-16 of Brown, an integrated circuit 10 receives a regulated power supply voltage V_{REG} generated by a voltage regulator 16. The regulator voltage V_{REG} is adjustable using a voltage adjustment signal, V_{ADJ}. The integrated circuit 10 includes a voltage adjustment circuit 22 (col. 3, lines 19-20), which can operate in two modes: a power determinate mode and an operating mode (col. 3, lines 22-24). In the power determinate mode, the voltage adjustment circuit 22 varies the value of the voltage adjustment signal V_{ADJ} over a predetermined range and, at discrete points in this range, a determination is made as to the overall operation of the

integrated circuit (col. 3, lines 24-29). In this regard, col. 3, lines 42-60 and col. 4, lines 4-14 describe the provision of a 25 MHz oscillator 30 coupled to ripple counters 36, 40, counter 48 and a latch 52. A ring oscillator 39 is also provided. As explained at col. 4, lines 14-18, the number of counts counted by the counter 48 is a function of the ring oscillator 39 and the propagation delay of each of the stages in the counter 48 and the count value represents a "gauge" for the speed of the system as a function of the voltage.

Returning to col. 3, lines 29-31, a table 24 is created for recording various operating characteristics gauged and associated values of V_{ADJ}.

In the operating mode (col. 3, lines 30-33), the voltage adjustment circuit 22 can accesses the voltage adjustment values V_{ADJ} stored and the highest count value recorded is identified (col. 4, lines 19-26) and the voltage adjustment value V_{ADJ} associated with the highest count value found is selected and set in order to ensure that the voltage regulator 16 provides the optimum operating power supply voltage (col. 4, lines 44-48, col. 5, lines 9-15 and lines 44-52).

Cited Borkar et al. also relates to control circuitry to control settings of a supply voltage signal and a clock signal to control a parameter of a processor, for example performance, power consumption and temperature (Abstract of Borkar et al.). Borkar et al. is primarily concerned with performance of transistors of an integrated circuit (col. 1, lines 13-17). According to col. 12, lines 30-33 cited by the Office Action, a performance rating of a domain (a region of transistors) can be determined for certain settings of supply voltage and body bias during pre-testing or actual use and stored in volatile or non-volatile memory in a chip. Col. 11, lines 11-14 clarifies that a performance rating signal can be thought of as a figure of merit as to how quickly the transistors of a group can switch and as such, the performance rating signal can be calibrated to a clock frequency for which the transistors of a group can switch acceptably.

Col. 13, lines 2-6, cited in the Office Action, explains that different techniques may be employed so as not to exceed power consumption levels, for example preventing a supply voltage not to exceed a certain level. Furthermore, col. 13, lines 25-30 discloses the use of a memory 290 to hold "signals indicating constraints on performance". Additionally, col. 13, lines 35-37 explain that control circuitry 262 of

Borkar et al. can provide the supply voltage so as to maintain temperature or a temperature range, and this strategy seems to be supported at col. 4, lines 34-42.

However, the objective of Borkar et al. is to achieve optimum performance (col. 12, lines 34-61) or optimum performance without unacceptable power consumption and heat (col. 12, line 62-col. 13, line 2). In this respect, the Office Action asserts (on page 5, lines 3-17 thereof) that Borkar et al. teaches a plurality of ranges. In view of this understanding, it is respectfully submitted that this is an incorrect assessment of Borkar et al., because col. 12, lines 29-32 refers to performance ratings and col. 11, lines 11-14 clarifies the definition of the term "performance rating", namely a single value, not a range. Indeed, Borkar et al. is silent as to the **storage** of multiple supply voltage values that **each** has a performance **range** associated therewith. Additionally, Borkar et al. does not identify the functional elements disclosed therein responsible for use of such ranges.

Referring to claim 1, claim 1 recites a device for regulating a voltage supply to a semiconductor device, said device comprising:

- a memory for storing a plurality of performance ranges, wherein each performance range of said plurality of performance ranges is associated with a respective different supply voltage and each performance range of said plurality of performance ranges has a performance limit of this semiconductor device associated therewith;
- a measuring function for measuring a performance of said semiconductor device;
- a reference circuit; and
- a regulator; wherein
- the memory, the reference circuit and the regulator are arranged to determine a lowest supply voltage required to maintain a performance of the semiconductor device at a given operational frequency and to modify the supply voltage to said semiconductor device if a measured performance of said semiconductor device is not within a predetermined portion of a performance range associated with said voltage supplied to said semiconductor device.

However, and with particular reference to the underlined feature of claim 1 above, the combination of cited Brown with Borkar et al. fails to teach the provision of a memory for storing a plurality of performance ranges, wherein each performance range of said plurality of performance ranges is associated with a respective different supply voltage and the memory, as recited in claim 1.

In reply to the specific points raised in numbered paragraph 8 on page 15 of the Office Action (Response to Arguments), it is argued that:

> "*Borker et al states that a supply voltage has a performance rating determined and stored in a memory (Borker, column 12, lines 29-33), and to maintain a performance rating different parameters may be adjusted (Borker, column 4, lines 53-56; column 12, lines 35-61), thus creating a plurality of performance ranges associated with a certain supply voltage and the voltage values associated with operational frequencies.*"

Applicants have difficulty following the logic employed in concluding: "thus creating a plurality of performance ranges associated with a certain supply voltage and the voltage values associated with operational frequencies". However, the Applicants interpret the above reasoning to mean that in order to maintain a performance rating different parameters may be adjusted, one of which, the supply voltage, can remain constant. If other parameters are mal-adjusted, the performance would vary, resulting in a range of performance ratings for a same supply voltage. If one extends this further, for a different supply voltage, there would be a different range of performance ratings. It is assumed that the Office Action asserts that such teachings are implied by Borker et al. However, the above cited passage from Borker fails to recognize a number of facts.

Firstly, Borker et al. actually suggests (col. 12, lines 29-33) that a supply voltage and body bias (i.e. a combination) may have performance ratings determined. In relation to data storage, col. 12, lines 29-33 of Borker et al. only refers to storage in this respect. It does not refer to storage in relation to a plurality of ranges being stored. Borker et al. simply mentions modifying supply voltage and body bias (col. 12, lines 35-61); no mention is made of storage of a plurality of ranges, each range corresponding to a respective supply voltage. The reference to col. 4, lines 53-56, is misleading, because

it relates not to maintenance of a performance rating, but to modification of performance in order to maintain **temperature** relative to certain parameters.

Brown only describes storage of parameters in respect of fixed intervals in a range of adjustment voltages V_{ADJ} (which relate to a regulated supply voltage, V_{REG}), each set of parameters associated with a single V_{ADJ} value relating to a single performance level. Hence, at best, this can be interpreted as storage of a single range of performance levels over a range of adjustment voltages.

Consequently, when one combines the disclosures of Brown and Borker et al., the combination still fails to teach storage of a plurality of performance ranges, as recited in claim 1. The combined documents only teaching storage of a single range of performance values over a range of supply voltages (Brown) or storage of something similar, namely the storage of multiple performance ratings for respective multiple supply voltage/body bias combinations.

In view of the reasoning provided above, Applicant submits that Brown in view of Borkar et al. does not render claim 1 obvious.

Claims 2 - 4, and 6-8 depend from claim 1. By virtue of this dependence, claims 2 - 4, and 6 - 8 are also not obvious.

Claim 9 is directed to a method for regulating a voltage supply to a semiconductor device and corresponds to the device of claim 1. Consequently, the arguments set forth above in support of claim 1 apply equally to claim 9. As such, it is therefore respectfully submitted that the combination of Brown with Borkar et al. fails to teach storing a plurality of performance ranges of the semiconductor device, wherein each performance range of said plurality of performance ranges is associated with a respective different supply voltage, as recited in claim 9.

In view of the reasoning provided above, Applicant submits that Brown in view of Borkar et al. does not render claim 9 obvious.

On page 7 of the Office Action, claims 5, and 10-30 are currently rejected under 35 USC § 103(a) as being unpatentable over US 5,847,552 (hereinafter referred to as “Brown”) and US 6,484,265 (hereinafter referred to as “Borkar et al.”) in view of US 6,996,730 (hereinafter referred to as “Bonnett”). Applicants are traversing this rejection.

Claims 5, and 10-18 are dependent upon independent claim 1. In view of the reasoning provided above in support of the patentability of independent claim 1, Applicants submit that claims 5, and 10-18 are allowable for this reason at least.

Likewise, claim 19 is dependent upon independent claim 9. In view of the reasoning provided above in support of the patentability of claim 9, Applicants submit that claim 19 is allowable for this reason at least.

As mentioned above, the application presently contains four independent claims, namely claims 1, 9, 20, and 30. Below, Applicants explain that Brown in combination with Bonnett do not teach all of the elements of claims 20 and 30.

Cited Bonnett relates to a method and apparatus for adjusting the clock frequency and voltage supplied to an integrated circuit (Abstract of Bonnett). As explained at col. 2, lines 36-39, a frequency detection circuit is provided that monitors a clock signal and causes a voltage regulator to raise the voltage supplied to the integrated circuit in response to the increased clock frequency.

The Office Action also refers to col. 5, lines 15-28, which explains that the PLL 310 generates a clock signal 314 that controls the operation of the processor 310 and that the PLL 310 receives “event signals” that instruct it either to speed up or slow down (col. 5, lines 19-20). Lines 20-22 of col. 5 describe a response by the PLL 310 to an “over temp signal” from a thermal detector that measures temperature of a megacell 300, and lines 26-28 of col. 5 explains that such events are used to control system clock speed. When read in combination with col. 2, lines 36-39, it seems that the voltage regulator would modify the voltage supplied to the integrated circuit in response to a change in the clock signal brought about by the PLL 310. However, this passage is silent as to the control of the voltage regulator 320 of Bonnett in relation to use of a temperature compensation voltage value. Indeed, Bonnett does not describe storage of multiple process temperature compensation voltage values where each such value is respectively associated with a different operational frequency.

Referring to claim 20, claim 20 recites a device for regulating a voltage supply to a semiconductor device, said semiconductor device comprising:

- a memory for storing a plurality of process temperature compensation voltage values, wherein each of said plurality process temperature compensation voltage

values are respectively associated with a different operational frequency for said semiconductor device; and

- a regulator for modifying said supply voltage to said semiconductor device if said operational frequency of said semiconductor device changes to a new operational frequency; wherein
- the memory stores a performance limit of the semiconductor device, the memory, the reference circuit and the regulator being arranged to determine a lowest supply voltage required to maintain a performance of the semiconductor device at a given operational frequency and modify said supply voltage to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency.

However, and with particular reference to the underlined feature of claim 20 above, the combination of cited Brown with Bonnett fails to teach the provision of a memory for storing a plurality of process temperature compensation voltage values, wherein each of said plurality process temperature compensation voltage values are respectively associated with a different operational frequency for said semiconductor device; and wherein the memory, the reference circuit and the regulator being arranged to modify said supply voltage to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency, as recited in claim 20.

The Office Action (page 7, lines 16-19) asserts that the skilled person "would recognize" that col. 2, lines 1-3, col. 4, lines 53-56, and col. 13, lines 35-38 of Borker et al. disclose a plurality of process temperature compensation voltages. However, Borker et al. does not disclose this feature and the Office Action has had to rely, respectfully, on tenuous "would recognize" logic.

In view of the reasoning provided above, Applicant submits that Brown and Borker et al. in view of Bonnett does not render claim 20 obvious.

Claims 21 – 29 depend from claim 20. By virtue of this dependence, claims 21 – 29 are also not obvious.

Claim 30 is directed to a method for regulating a voltage supply to a semiconductor device and corresponds to the device of claim 20. Consequently, the arguments set forth above in support of claim 20 apply equally to claim 30. As such, it is therefore respectfully submitted that the combination of Brown, Borker et al. and Bonnett fails to teach storing a plurality of process temperature compensation voltage values, wherein each of said plurality of process temperature compensation voltage values are respectively associated with a different operational frequency for said semiconductor device; and modifying said supply voltage to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency, as recited in claim 30.

In view of the reasoning provided above, Applicant submits that Brown in view of Bonnett does not render claim 30 obvious.

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim are provided without addressing these statements. Therefore, Applicants reserve the right to address these statements at a later time if necessary.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

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